Factsheet

IEEE 1394a eVC – SI170FWA*e*V20

Silicon Cores™

Core to the Intelligent System™

*e*VC IEEE 1394a-2000 Link Layer Controller VIP

Silicon Interfaces' IEEE 1394a-2000 Link Layer Controller *e*VC is a fully documented, off the shelf component for Cadence Specman Elite™ functional verification environment.

The IEEE 1394 a-2000 link layer controller (from now on referred to only as 1394a) provides connectionless acknowledged data transfer services between a source node and destination node where node is an addressable device attached to the serial bus with at least a minimum set of control registers.

*e*VCs are configurable, reusable verification components written in the *e* language and designed to simplify and speed up the verification tasks. These comprise a complete verification environment including stimulus generation, checking, monitoring and functional coverage. *e*VCs provide major increase in the productivity and higher quality products.

The IEEE 1394a Function Controller *e*VC verifies designs that include IEEE 1394a Function Controller. This *e*VC accurately verifies and ensures that the particular function controller is satisfying the IEEE 1394a protocol, as well as thoroughly exercises the link controller.

The *e*VC supports IEEE 1394a PHY specification at the Physical side and Transaction Layer specification at the Host side. Data transmission can be configured to be at 100, 200 or 400 Mbps and can also be configured to be asynchronous or isochronous transaction.

Product Highlights

- ☑ Fully compliant with the IEEE 1394a specifications
- ☑ Totally configurable, as per user requirements
- ☑ Can operate at 100 Mbps, 200Mbps and 400 Mbps
- ☑ Supports IEEE 1394a PHY interface at Physical side and Application, Transaction layer and Serial Bus Manager features at the Host side
- ☑ Protocol Compliance checking
- ☑ Can be configured to be in root and non-root mode to check generation and reception of cycle start packet
- ☑ Random generation of Asynchronous and Isochronous data packets
- ☑ Covers all types of transaction
- ☑ Compares driven data packets with received data packets
- ☑ Computing CRC of data packets

Provides CRC error notification

- ☑ Configuration and reading of CSR's
- ☑ The IP monitors the various transactions and their sequences.
- ☑ Perl script makes configuration easier
- ☑ HDL independent.

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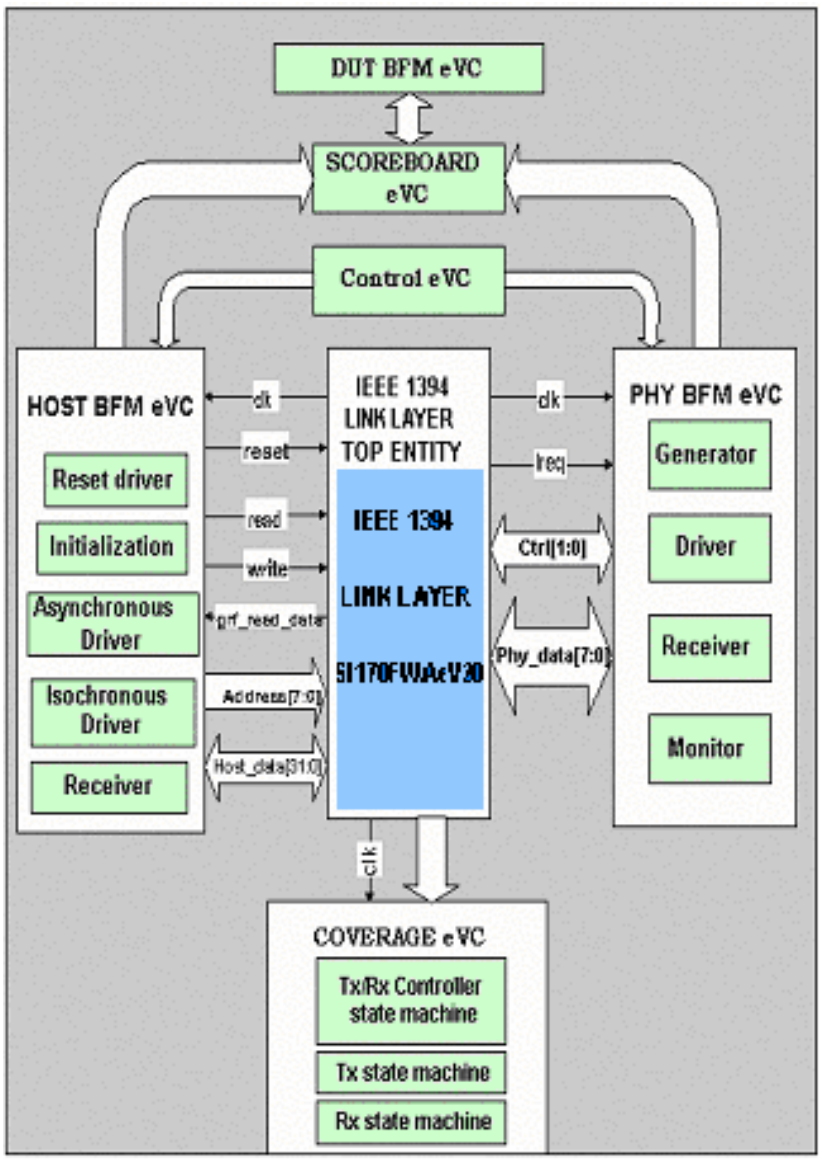
IEEE 1394a Block Representative Schematic



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Verification Methodology:

An IEEE 1394a Link Layer Controller *e*VC initiates the IEEE 1394a PHY layer and Transaction and Application layer compliant transactions. These transactions are applied to the Device under Test (DUT) and as well as to the *e*VC Device.

The PHY BFM is a model of the PHY layer of the protocol, which on one side interfaces with the link layer (SI70FW11) and on the other side with the serial bus. The HOST BFM emulates the Transaction layer, Application layer and the Serial Bus Manager features. Both the HOST and the PHY BFM's generate, transmit and receive Protocol data units.

The data checker, which is implemented in the form of scoreboard, compares the data collected at the HOST or the PHY receiver with the data driven from the PHY or HOST transmitter respectively, thus verifying adherence to the IEEE 1394a protocol.

At all the times the *e*VC monitors signals at the HOST and PHY Bus function model interface. Coverage block covers all the states defined in the DUT main state machines and reports whenever an illegal transition occurs.

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